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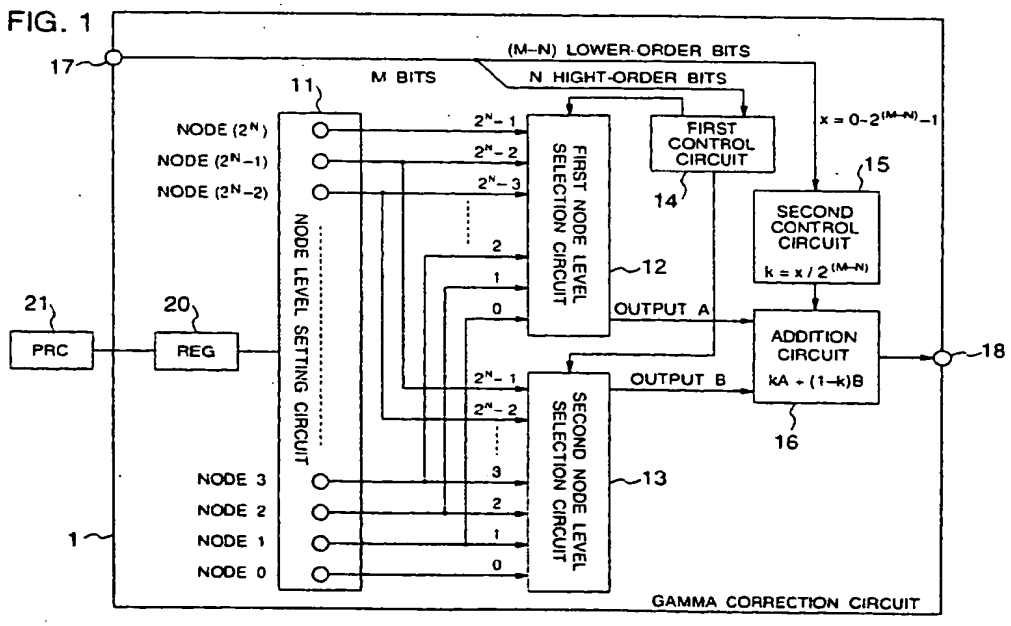
(54) Gamma correction circuit

(57) In a gamma correction circuit some bits of the digital data to be converted are used to select two gamma corrected "node" voltages. The other bits are used to make a linear interpolation between the two voltages using an addition circuit.

In order to adapt the gamma correction circuit to a specific display panel, the set of "node" voltages can be programmed.

FIG. 1



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Description

[0001] The present invention relates to a gamma correction circuit for implementing favorable gradation and contrast of reproduced images in display devices such as a liquid crystal display device (hereinafter referred to as LCD), a plasma display panel (hereinafter referred to as PDP) and a digital micromirror device (hereinafter referred to as DMD).

[0002] In recent years, display devices such as LCDs, PDPs and DMDs have attracted attention. Gamma characteristics of these new display devices are different from characteristics of the cathode-ray tube (hereinafter referred to as CRT) type heretofore used. In addition, display devices such as LCDs, PDPs and DMDs have also different characteristic, respectively.

[0003] Furthermore, in current television broadcast, the gamma correction is conducted on an image transmitting side so as to cancel the gamma characteristic of a display side by supposing that the display device uses a CRT.

[0004] In the case where a LCD, a PDP or a DMD is used as display device, it is necessary to correct the gamma characteristic of the image transmitting side and simultaneously therewith correct the gamma characteristic of each of display devices such as LCDs, PDPs or DMDs.

[0005] As for a circuit for implementing such gamma correction having a variable characteristic, the circuit typically includes a look up table (hereinafter referred to as LUT) for specifying a predetermined characteristic by using a ROM or the like as described, for example, in JP-A-8-190363 and JP-A-8-194450 as laid-open gazette.

[0006] A gamma correction circuit 100 using a LUT shown in FIG. 3 includes input terminals 101 to 103 respectively supplied with image signals of three systems, i.e., R (Red), G (Green) and B (Blue) before gamma correction, processing circuits 111 to 113 for correcting gamma characteristics respectively for the systems of R, G and B, LUTs 121 to 123 each having a plurality of LUTs for storing beforehand gamma characteristic conformed to display devices, a control circuit 130 for selecting one of the plurality of LUTs for each of LUTs 121 to 123 of the respective systems in conformity with the gamma characteristic of the display device, and output terminals 141 to 143 for outputting image signals after gamma correction. The LUTs 121 to 123 are stored in a ROM 120. As exemplified by the R system, the plurality of LTUs 121-1 to 121-n storing different gamma characteristics are included.

[0007] In the gamma correction circuit 100 having LUTs as shown in FIG. 3, as many tables as corresponding gamma characteristics must be prepared. In addition, it is necessary to determine the gamma characteristic and store it in the ROM beforehand. Therefore, for obtaining a gamma correction circuit corresponding to a plurality of display devices differing in gamma characteristic, such as a CRT, LCD, PDP and DMD, and corresponding to a signal subject to gamma correction beforehand, such as a TV signal, and a plurality of signals which have not been subjected to gamma correction, such as PC (personal computer) signals, the circuit scale becomes large. It is not easy to alter the gamma characteristic from the outside.

[0008] An object of the present invention is to provide a gamma correction circuit capable of altering the gamma correction characteristic according to the gamma characteristic of the display device and capable of altering the gamma correction characteristic according to the input signal, by using a small circuit scale.

[0009] In accordance with the present invention, a gamma correction circuit includes a node level setting unit and a gamma correction unit. An encoded M-bit (where M is an arbitrary integer) video signal is represented by using a predetermined number of sections. Level values of the video signal predetermined so as to be respectively associated with $2^n + 1$ number of nodes (where n is an arbitrary integer) respectively determined for the sections are set in the node level setting unit from an outside. The gamma correction unit executes gamma correction of the M-bit video signal according to level values of the nodes set in the node level setting unit.

[0010] On a gamma characteristic curve representing the encoded M-bit video signal by using 2^n number of sections, a level of the video signal in the M sections is represented by using the $2^n + 1$ number of nodes. In this case, level values of the video signal predetermined so as to be respectively associated with the nodes can be set in the node level setting unit from the outside.

[0011] The gamma correction unit may include a selection circuit supplied with level values of the 2^n number of nodes from the node level setting unit. The selection circuit selects and outputs a level value of a start point and a level value of an end point of each of segments virtually connected between nodes, out of the $2^n + 1$ number of level values specified by the node level setting unit.

[0012] The selection circuit may includes a first selection circuit and a second selection circuit each supplied with level values of 2^n number of nodes from the node level setting unit. The first selection circuit and the second selection circuit respectively select and output the level value of the start point and the level value of the end point of each of segments virtually connected between the nodes, out of the $2^n + 1$ number of level values specified by the node level setting unit.

[0013] The gamma correction unit may include a first control circuit for controlling the first and second selection circuits by using a value of N high-order bits (where N is an arbitrary integer) specifying the segment out of the M-bit video signal inputted from the video signal input terminal.

[0014] The gamma correction unit may include an addition circuit for calculating a mixture ratio, according to which level values of the end point and the start point

outputted from the first and second selection circuits are mixed, by using a coefficient and predetermined computation, and generating a gamma corrected video signal.

[0015] The gamma correction unit may include a second control circuit for calculating the coefficient from a value of (M - N) low-order bits included in the M-bit video signal inputted from the video signal input terminal, by predetermined computation.

[0016] The node level setting unit may be connected to shift registers storing beforehand level values indicating the nodes, and the level values may be inputted from the shift registers to the node level setting unit.

[0017] The shift registers may be connected to a microprocessor, and level values of the nodes may be indicated from the microprocessor according to a characteristic of the display device.

[0018] The first control circuit may specify the segment by a value of N high-order bits out of the M-bit video signal, cause the first selection circuit to output a level value of a start point of the segment, and cause the second selection circuit to output a level value of an end point of the segment.

[0019] The node level setting unit and the gamma correction unit may be provided in a circuit of each of R system, B system and G system.

[0020] In the drawings

FIG. 1 is a block diagram showing the configuration of a gamma correction circuit according to the present invention;

FIG. 2 is a diagram showing an example of gamma characteristics which can be implemented by the present invention; and

FIG. 3 is a block diagram showing the configuration of a gamma correction circuit which is an example of related art.

[0021] Hereinafter, an embodiment of the present invention will be described by referring to drawing. FIG. 1 is a block diagram showing an embodiment of a gamma correction circuit according to the present invention.

[0022] With reference to FIG. 1, a gamma correction circuit 1 includes a node level setting circuit 11 for specifying at least $2^n + 1$ number of node level values, where n is an arbitrary integer, a first node level selection circuit 12 supplied with 2^n number of level values for selecting a segment end point out of the $2^n + 1$ number of level values set by the node level setting circuit 11, a second node level selection circuit 13 supplied with the 2^n number of level values for selecting a segment start point out of the $2^n + 1$ number of level values set by the node level setting circuit 11, a video signal input terminal 17 for inputting a video signal before the gamma correction encoded in M bits, where M is an arbitrary integer, a first control circuit 14 for controlling the first node level selection circuit 12 and the second node level selection circuit 13 by using a value of N high-order bits specifying a segment out of M-bit data inputted from the video signal input terminal 17, where N is an arbitrary integer, a second control circuit 15 for outputting a coefficient for controlling a mixture ratio of level values respectively of a start point and an end point by using an adder 16 and a value of (M - N) low-order bits of an M-bit video signal inputted from the video signal input terminal 17, the adder 16 for adding outputs of the first node level selection circuit 12 and the second node level selection circuit 13 with a mixture ratio altered by the coefficient supplied from the second control circuit 15, and a video signal output terminal 18 for outputting an output signal of the adder 16 after gamma correction.

[0023] Here, nodes and segments will be described. As shown in FIG. 2, predetermined gamma characteristic curves are supposed. Assuming now that a video signal inputted from the video signal input terminal 17 is represented by eight bits and the video signal is divided into eight sections by using three high-order bits included in the eight bits, there are number $2^3 + 1$ of partitions. Points existing on these partitions and each represented by an input level value and an output level value of a video signal are referred to as nodes. Each of lines virtually connecting nodes is referred to as segment. In each segment, a node indicating a low level value is referred to as start point, and a node indicating a high level value is referred to as end point.

[0024] FIG. 2 shows an example of the gamma characteristic obtained in the present embodiment. Black dots indicate output level values which can be specified at respective nodes. A gamma characteristic curve formed of eight segments can be implemented. This gamma characteristic shows an example in which gamma characteristics of the three systems, i.e., R, G and B are corrected independently. It is possible to specify gamma characteristics independently and respectively for the systems of R, G and B.

[0025] By taking as an example, the case where a video signal encoded in eight bits (M = 8) is inputted from the video signal input terminal 17 and the gamma characteristic of eight nodes (N = 3) is implemented, operation of the gamma correction circuit 1 of, for example, the R system will now be described.

[0026] Output level values (set level values) of nine ($= 2^3 + 1$) nodes drawing a predetermined gamma characteristic curve shown in FIG. 2 and ranging from node 0 to node 8 are specified in the node level setting circuit 11 by using eight bits for each of the nodes. This can be implemented by, for example, specifying level values in nine eight-bit shift registers 20. Furthermore, by connecting the shift registers 20 to a microprocessor 21 and setting level values corresponding to nodes of display devices differing in characteristic, such as a LCD, PDP and DMD, from the microprocessor, gamma correction can be implemented. Although the level values can be set from the outside, it is not always necessary to make all of the nine nodes variable.

[0027] As for the gamma characteristic curve set in

the node level setting circuit 11, the axis of abscissas represents an input level value and the axis of ordinates represents an output level value, and the gamma characteristic curve is represented by eight segments connecting nine nodes.

[0028] The eight segments 1 to 8 have three high-order bits equivalent to "000", "001", "010", "011", "100", "101", "110" and "111", respectively. As for output level values of nine nodes (nodes 0 to 8), for example, output level values of the nodes 0 to 7 can be made values at points where the input level has five low-order bits "00000", and an output level value of the node 8 can be made a value at a point where the input level has five low-order bits "11111".

[0029] Among node level values outputted from the node level setting circuit 11, level values of end points of the node 8 to node 1 are inputted respectively to points of the first node level selection circuit 12 associated with three high-order bits, and level values of start points of the node 0 to node 7 are inputted respectively to points of the second node level selection circuit 13 associated with the three high-order bits. The level value of the first node level selection circuit 12 specifies the output level value of the end point of each segment. The level value of the second node level selection circuit 13 specifies the output level value of the start point of each segment.

[0030] Among the eight bits of the video input signal inputted from the video signal input terminal 17, three high-order bits are inputted to the first control circuit 14. By controlling the first node level selection circuit 12, the first control circuit 14 selects an output level value "A" of an end point of a segment included in the eight segments and associated with input data of the three high-order bits. By controlling the second node level selection circuit 13, the first control circuit 14 selects an output level value "B" of a start point of a segment included in the eight segments and associated with input data of the three high-order bits.

[0031] Among the eight bits of the video input signal inputted from the video signal input terminal 17, five-low order bits are inputted to the second control circuit 15. A value x of the five bits is in the range of $x = 0$ to $(2^5 - 1)$. From the inputted five low-order bits, the second control circuit 15 generates a coefficient $k = x / 2^5$.

[0032] To the addition circuit 16, there are inputted the output signal A of the end point selected by the first node level selection circuit 12, the output signal B of the start point selected by the second node level selection circuit 13, and the coefficient k supplied from the second control circuit 15.

[0033] By using the coefficient k supplied from the second control circuit 15 and the output signals A and B supplied from the node level selection circuits 12, 13, the adder 16 conducts computation in accordance with an expression of $kA + (1 - k) B$, and specifies an output level value between the start point and the end point of each segment.

[0034] An output signal computed by the adder 16 is outputted from the video signal output terminal 18. A video output is thus obtained after gamma correction.

[0035] The case where an eight-bit video signal of "01110101" is inputted to the gamma correction circuit 1 will now be described. For the segment 4 having the three high-order bits "011", it is now assumed that the output level value of the node 3 is set to "90" and the output level value of the node 4 is set to "120". It then follows that $x = 21$, $k = 21/32$, $A = 120$, and $B = 90$. Therefore, the output of the adder 16 becomes approximately 110.

[0036] As described above, the gamma correction circuit 1 is formed of the node level setting circuit 11 supplied with the number (M) of bits of the video signal plus 1 (= M + 1) data, the two node level selection circuits 12 and 13, the two control circuits 14 and 15, and the adder 16. As a result, correction of the gamma characteristic can be conducted on the video input signal.

[0037] Furthermore, since the gamma characteristic of this gamma correction circuit 1 can be easily altered by rewriting the node level setting circuit 11, the gamma correction circuit 1 corresponding to a display device, such as a LCD, PDP, and DMD, can be obtained.

[0038] In the foregoing description, an example in which correction of the gamma characteristic is conducted for the R system has been shown. It is also possible to provide gamma correction circuits for the G system and the B system as well and conduct gamma correction for the R, G and B systems respectively and independently. Alternatively, it is also possible to use one gamma correction circuit and provide the three systems of R, G and B with the same gamma characteristic.

[0039] The gamma correction circuit shown in FIG. 1 can be incorporated as a one-chip LSI. By incorporating it in display devices of all different types, video images corresponding to the video transmitting side can be displayed. It is a matter of course that the shift registers 20 and the microprocessor 21 can also be incorporated into the one-chip LSI.

Claims

1. A gamma correction circuit for providing gamma correction for each of display device and input signal, comprising:

   a node level setting means (11) set predetermined level values of video signals from outside, in a case where encoded M-bit (where M is an arbitrary integer) video signals being represented by using predetermined number of sections and the level values of the video signals corresponding to $2^n + 1$ number of nodes (where n is an arbitrary integer) associated with the sections on which the nodes are specified; and

a gamma correction means (12, 13, 14, 15, 16) for executing gamma correction of the M-bit video signal in accordance with the level values of the nodes set in said node level setting means.

2. A gamma correction circuit according to claim 1, wherein

said node level setting means (11) is set the predetermined level values of the video signals from the outside such that the level values correspond to the nodes, in a case where the levels of the video signals associated with 2^n number of sections being represented by the $2^n + 1$ number of nodes on a gamma characteristic curve representing the encoded M-bit video signal by using the number of 2^n sections.

3. A gamma correction circuit according to claim 2, further comprising a video signal input terminal (17) for inputting the video signal encoded in M bits.

4. A gamma correction circuit according to claim 1, wherein the gamma correction means (12, 13, 14, 15, 16) includes a selection circuit (12, 13) receiving the level values corresponding to the 2^n number of nodes from said node level setting means (11), and selecting a level value of a start point and a level value of an end point of segments virtually connected between the nodes associated with the $2^n + 1$ number of level values specified by said node level setting means to output the level values.

5. A gamma correction circuit according to claim 4, wherein said selection circuit (12, 13) includes: a first selection circuit (12) receiving the level values corresponding to the 2^n number of nodes from said node level setting means (11), and selecting the level value of the start point of the segments virtually connected between the nodes associated with the $2^n + 1$ number of level values specified by said node level setting means to output the level value of the start point, and

a second selection circuit (13) receiving the level values corresponding to the 2^n number of nodes from said node level setting means (11), and selecting the level value of the end point of the segments virtually connected between the nodes associated with the $2^n + 1$ number of level values specified by said node level setting means to output the level value of the end point.

6. A gamma correction circuit according to claim 5, wherein said gamma correction means includes a first control circuit (14) for controlling said first and second selection circuits (12, 13) by using a value of N high-order bits (where N is an arbitrary integer) specifying the segment out of the M-bit video signal inputted from the video signal input terminal.

7. A gamma correction circuit according to claim 6, wherein said gamma correction means includes an adder (16) for calculating a mixture ratio, according to which the level values of the end point and start point outputted from said first and second selection circuits (12, 13) are mixed, by using a coefficient and predetermined computation, and generating a gamma corrected video signal.

8. A gamma correction circuit according to claim 7, wherein said gamma correction means includes a second control circuit (15) for calculating the coefficient from a value of (M - N) low-order bits included in the M-bit video signal inputted from the video signal input terminal, by predetermined computation.

9. A gamma correction circuit according to claim 7, wherein said adder includes a video signal output terminal (18) for outputting the gamma corrected video signal.

10. A gamma correction circuit according to claim 7, wherein said node level setting means (11) is connected to a shift register storing beforehand the level values indicating the nodes, and the level values are inputted from said shift register to said node level setting means (11).

11. A gamma correction circuit according to claim 10, wherein said shift register (20) is connected to a microprocessor (21), and the level values of the nodes are indicated from said microprocessor in accordance with a characteristic of a display device.

12. A gamma correction circuit according to claim 10, wherein said first control circuit (14) specifies the segment by a value of N high-order bits out of the M-bit video signal, causes said first selection circuit to output the level value of the start point of the segment, and causes said second selection circuit to output the level value of the end point of the segment.

13. A gamma correction circuit according to claim 1, wherein said node level setting means (11) and said gamma correction means (12, 13, 14, 15, 16) are provided in each circuit of R-system, B-system and G-system.

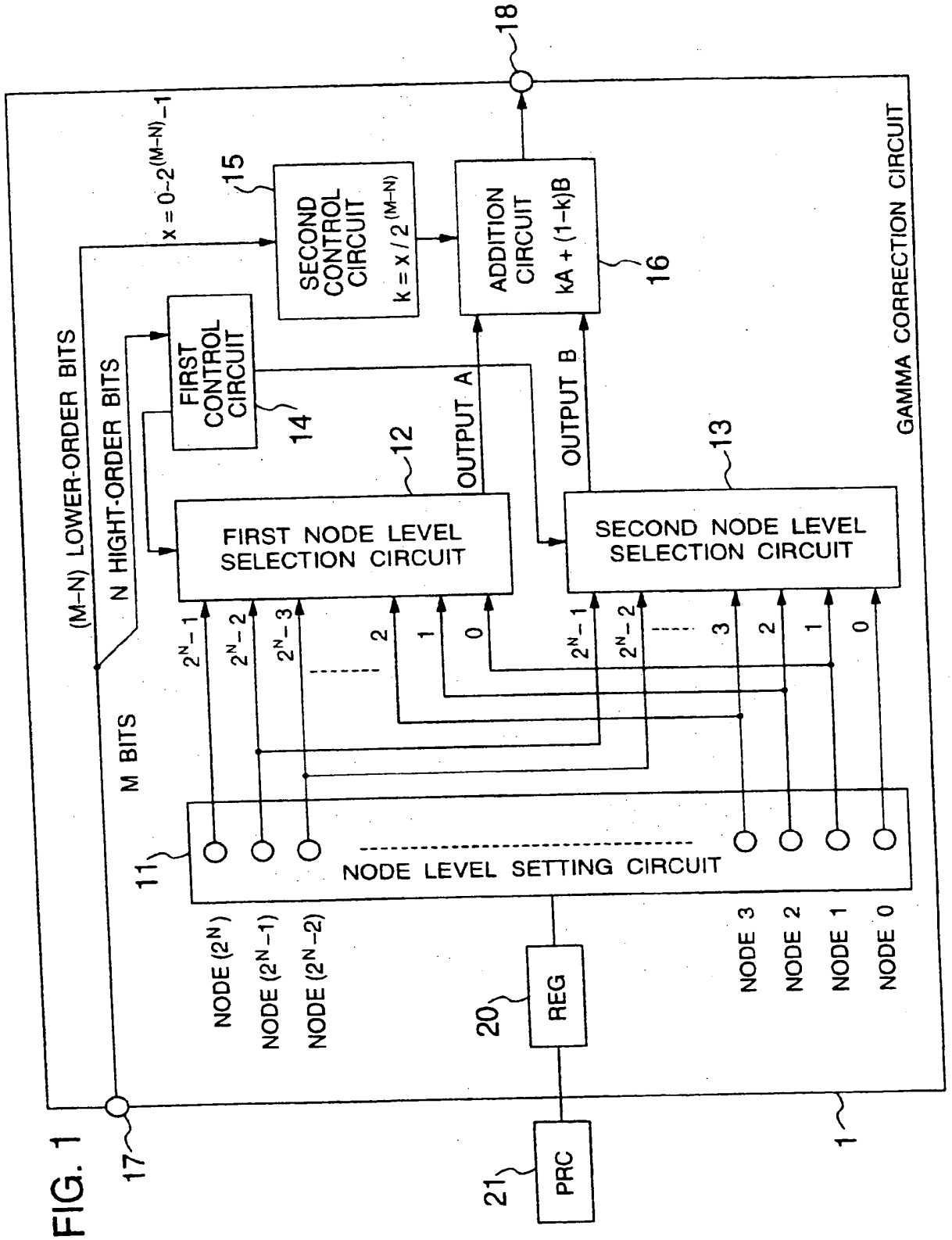

GAMMA CORRECTION CIRCUIT
(M-N) LOWER-ORDER BITS
N HIGHT-ORDER BITS
M BITS
x = 0~2^(M-N)-1
SECOND CONTROL CIRCUIT
k = x / 2^(M-N)
ADDITION CIRCUIT
kA + (1-k)B
FIRST CONTROL CIRCUIT
OUTPUT A
OUTPUT B
FIRST NODE LEVEL SELECTION CIRCUIT
SECOND NODE LEVEL SELECTION CIRCUIT
NODE LEVEL SETTING CIRCUIT
NODE (2^N)
NODE (2^N-1)
NODE (2^N-2)
NODE 3
NODE 2
NODE 1
NODE 0
REG
PRC
18
15
16
14
12
13
11
20
21
17
1

FIG. 1

FIG. 2

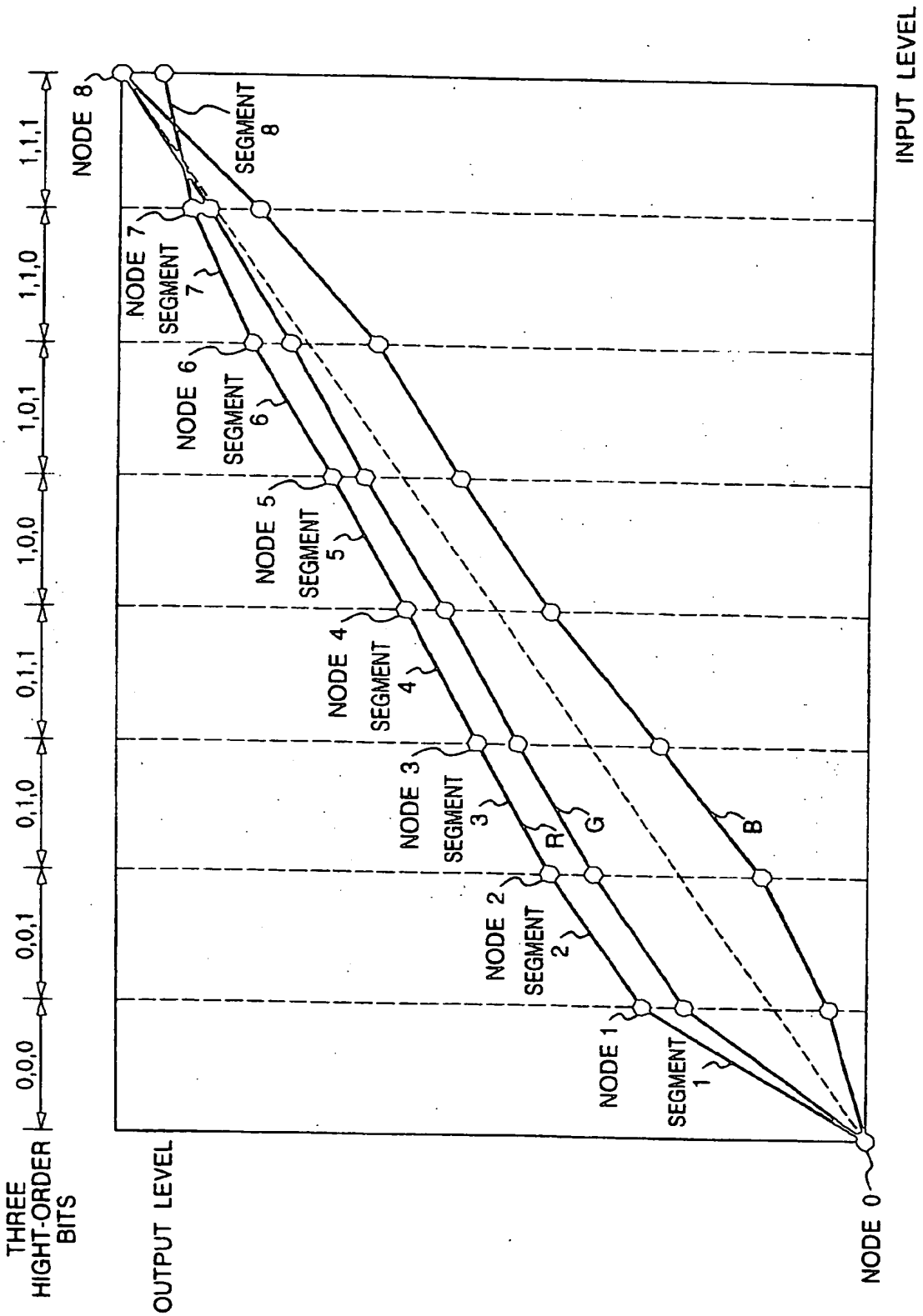
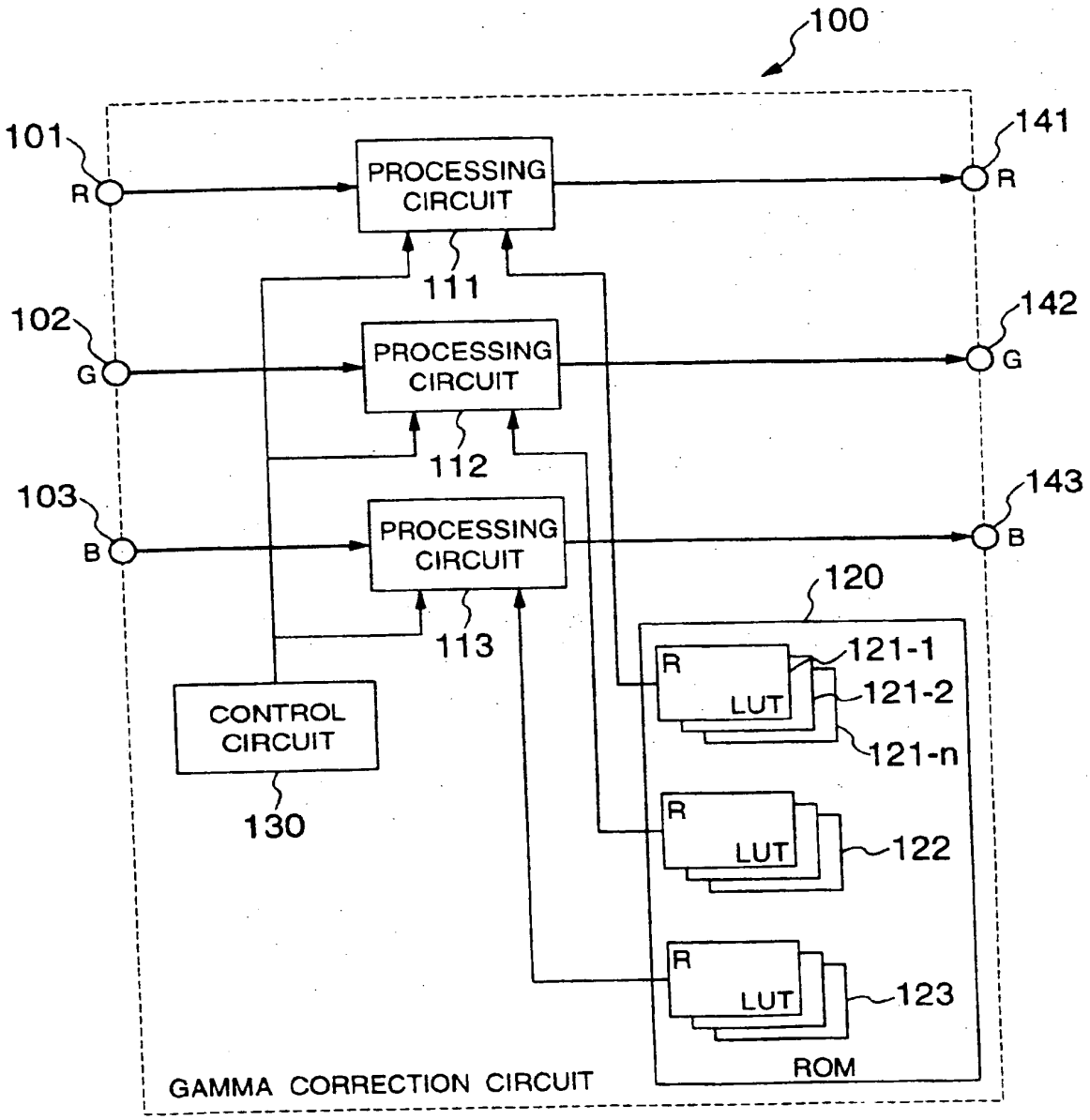


FIG. 3


100
101
R
PROCESSING CIRCUIT
141
R
111
102
G
PROCESSING CIRCUIT
142
G
112
103
B
PROCESSING CIRCUIT
143
B
120
113
R
LUT
121-1
121-2
121-n
CONTROL CIRCUIT
130
R
LUT
122
R
LUT
123
ROM
GAMMA CORRECTION CIRCUIT

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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 2559

DOCUMENTS CONSIDERED TO BE RELEVANT

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A	* page 5, line 25 - page 6, line 22 * * page 8, line 21 - page 9, line 24 * * page 11, line 3 - page 12, line 30 * * page 14, line 30 - page 15, line 8 * * figures 4-7 *	10,11	
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A	* column 22, line 56 - column 24, line 22; figures 4,13 *	7-9,12	
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TECHNICAL FIELDS SEARCHED (Int.Cl.6)
G09G
H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 July 1999	Amian, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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15-07-1999

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